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Docket No.: 08211/0200390-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Hon Kin Chiu

Patent No.: 6,834,093

Issued: December 21, 2004

For: FREQUENCY COMPARATOR CIRCUIT

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322 AND 37 CFR 1.322

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted which should be corrected.

The following errors were not in the application as filed by applicant:

In the Application:

Column 3, Line 45, Delete "[fIN2-**fIN**])" and insert - - [fIN2-**fIN1**]) - -.

Column 4, Line 45, Delete "ar**c**" and insert - - ar**e** - -.

Column 4, Line 62, Delete "(1/fIN2-**1**fIN1)" and insert - - (1/fIN2-**1/f**IN1) - -.

Column 7, Line 54, In Claim 12, delete "second input" and insert -- second output --.

Column 8, Line 27, In Claim 17, delete "the clock" and insert -- a clock --.

Column 8, Line 28, In Claim 17, delete "the clock" and insert -- a clock --.

Enclosed please find copies of pages 5, 6, 12 & 13.

The following errors were found in the application as filed by applicant. The errors now sought to be corrected are inadvertent typograpical errors, the correction of which does not involve new matter or require reexamination.

Column 4, Line 28, Delete "1/FIN1" and insert - - 1/fIN1 - -.

Column 4, Line 38, Delete "1/FIN2" and insert - - 1/fIN2 - -.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction. Enclosed please find a check for $100.00.

Dated: May 12, 2005

Respectfully submitted,

By _____

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	6,834,093
APPLICATION NO.	:	10/804,866
ISSUE DATE	:	December 21, 2004
INVENTOR(S)	:	Hon Kin Chiu

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Application:

Column 3, Line 45, Delete "[fIN2-fIN])" and insert - - [fIN2-fIN1]) - -.

Column 4, Line 28, Delete "1/FIN1" and insert - - 1/fIN1 - -.

Column 4, Line 38, Delete "1/FIN2" and insert - - 1/fIN2 - -.

Column 4, Line 45, Delete "arc" and insert - - are - -.

Column 4, Line 62, Delete "(1/fIN2-1fIN1)" and insert - - (1/fIN2-1/fIN1) - -.

Column 7, Line 54, In Claim 12, delete "second input" and insert -- second output --.

Column 8, Line 27, In Claim 17, delete "the clock" and insert -- a clock --.

Column 8, Line 28, In Claim 17, delete "the clock" and insert -- a clock --.

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embodiments, AND gate A1 may be replaced with another circuit that is configured to provide signal Status using the same truth table as an AND gate, and the like. In one embodiment, tol1 is substantially given by fIN1/(M1*[fIN1-fIN2]), where M1 is the maximum count value of counter circuit 110. Similarly, in one embodiment, tol2 is substantially given by fIN2/(M2*[fIN2-fIN1]), where M2 is the maximum count value of counter circuit 111.

In one embodiment, tol1 and tol2 provide the tolerance window, where tol1 is an upper tolerance value for fIN1, and tol2 is a lower tolerance value for fIN1.

In one embodiment, frequency comparator circuit 100 may used for charge pump control in a phase-locked loop. In one embodiment, if signal Status is high, the charge pump provides nominal current. In this embodiment, if signal Status is low, the charge pump current is increased to speed up acquisition time.

FIGURE 2 shows a block diagram of an embodiment of frequency detector circuit 220. Frequency detector circuit 220 may operate in a substantially similar manner as frequency detector circuit 120, and may operate differently in some ways. Frequency detector circuit 220 includes flip-flops FF201-FF204 and a clear logic circuit. In one embodiment, the clear logic circuit includes delay circuits DL201-DL203, NAND gate NAND201, inverter INV201, and multiplexer MX201.

The clear logic circuit may be arranged to activate a clear signal (CLR) if signal Q301 and signal RSTA correspond to a first logic level, and arranged to deactivate signal CLEAR if at least one of signal Q301 and signal RSTA corresponds to a second logic level. FF201 may be arranged to set signal Q301 to the first logic level in response to signal IN1 if signal CLEAR is deactivated, and arranged to reset signal Q301 to the second logic level if signal CLEAR is activated. FF202 may be arranged to set signal RSTA to the first logic level in response to signal IN2 if signal CLEAR is deactivated, and arranged to reset signal RSTA to the second logic level if signal CLEAR is activated. FF203 may be arranged to activate signal RSTA in response to signal IN1 if signal Q301 corresponds to the first logic level, such that signal RSTA is activated if signal IN1 pulses twice before signal CLEAR is activated. FF204 may be arranged to activate signal RSTB in response to signal IN2 if signal RSTA corresponds to the first logic level, such that signal RSTB is activated if signal IN2 pulses twice before signal CLEAR is activated.

Frequency detector circuit 220 is arranged such that signals RSTA and RSTB are dependent on fIN1 and fIN2, and such that signals RSTA and RSTB are substantially independent of the phases of signals IN1 and IN2.

If fIN1 ≥ fIN2, fRSTB is substantially zero. Similarly, if fIN1 ≤ fIN2, fRSTA is substantially zero.

If 2*fIN2>fIN1>fIN2, then fRSTA is substantially given by fIN1-fIN2, and the duty cycle of signal RSTA is substantially 50%. If fIN1>2*fIN2, signal RSTA behaves in a similar manner, except that, occasionally, a pulse of signal RSTA has a pulse duration of 2/fIN1 instead of 1/FIN1. If fIN1>>fIN2, fRSTA is substantially the same as fIN2, and the duty cycle of signal RSTA is substantially given by (fIN1-fIN2)/fIN1.

Similarly, if 2*fIN1>fIN2>fIN1, then fRSTB is substantially given by fIN2-fIN1, and the duty cycle of signal RSTB is substantially 50%. If fIN2>2*fIN1, RSTB behaves in a similar manner, except that, occasionally, a pulse of signal fRSTB has a pulse duration of 2/fIN2 instead of 1/FIN2. If fIN1<<fIN2, fRSTB is substantially the same as fIN1, and the duty cycle of signal RSTB is substantially given by (fIN2-fIN1)/fIN2.

Referring back to FIGURE 1, in one embodiment, circuit 100 includes counter circuits 110 and 111, further includes frequency detector circuit 220 as an embodiment of frequency detector circuit 120, and counter circuits 110 and 111 are both C bit counters. In this embodiment, if fIN1 and fIN2 are within a $1/2^C$ tolerance of each other, signal Status is high. Otherwise, signal Status is low. This may be more readily understood through the following mathematical calculations.

If 2*fIN2>fIN1>fIN2, in order for a pulse to occur in signal RSTA for a duration of (N -1) pulses of signal IN2, at least N pulses must occur in signal IN1. The Nth pulse of signal IN1 must happen sooner than the (N-1)th pulse of signal IN2 in order to propagate a logic 1 at signal RSTA (i.e. two consecutive pulses of signal IN1 with no pulse of signal IN2 in between).

Accordingly, $N * TA < (N - 1) * TB$, where TA and TB are the periods of signal IN1 and signal IN2 respectively.

$$\Rightarrow \quad TB < N * TB - N * TA$$

$$\Rightarrow \quad TB / (TB - TA) < N$$

$$\Rightarrow \quad (1/fIN2) / (1/fIN2 - 1/fIN1) < N$$

12. A frequency comparator circuit, comprising:

a frequency detector circuit having at least first and second inputs, and first and second outputs;

a first counter circuit having at least a clock input that is coupled to the first input of the frequency detector circuit, and a clear input that is coupled to the first input of the frequency detector circuit;

a second counter circuit having at least a clock input that is coupled to the second input of the frequency detector circuit, and a clear input that is coupled to the second input of the frequency detector circuit.

13. The frequency comparator circuit of Claim 12, further comprising an AND circuit that is coupled to the first and second counter circuits.

14. The frequency comparator circuit of Claim 12, further comprising an AND gate having a first input that is coupled to an overflow output of the first counter circuit, and a second input that is coupled to an overflow output of the second counter circuit.

15. The frequency comparator circuit of Claim 12, wherein the frequency detector circuit is configured to receive first and second input signals at the first and second inputs, a first frequency is associated with the first input signal, a second frequency is associated with a second input signal, and wherein the frequency detector circuit is further configured to provide first and second reset signals at the first and second outputs such that, if the first and second frequencies are relatively close:

if the first frequency is greater than the second frequency, the first reset signal includes a first parameter that is related to a difference between the first and second frequencies, and

if the first frequency is less than the second frequency, the second reset signal includes a second parameter that is related to the difference between the first and second frequencies.

16. The frequency comparator circuit of Claim 12, wherein the frequency detector circuit includes four flip-flops and a clear logic circuit.

17. The frequency comparator circuit of Claim 12, wherein the first counter circuit includes:

a register circuit; and

a flip-flop that is arranged to store an overflow condition related to the register circuit, and

wherein the frequency comparator circuit further includes a delay circuit that is coupled between the clock input of the frequency detector circuit and the clock input of the register circuit.

18. The frequency comparator circuit of Claim 12, wherein the frequency detector circuit includes:

a first flip-flop circuit having a clock input that is coupled to the clock input of the first counter circuit;

a second flip-flop circuit having a clock input that is coupled to the clock input of the second counter circuit;

a third flip-flop circuit having a clock input that is coupled to the clock input of the first counter circuit, another input that is coupled to an output of the first flip-flop circuit, and an output that is coupled to the clear input of the first counter circuit;

fourth flip-flop circuit having a clock input that is coupled to the clock input of the second counter circuit, another input that is coupled to an output of the second flip-flop circuit, and an output that is coupled to the clear input of the second counter circuit; and

a clear logic circuit having a first input that is coupled to the output of the first flip-flop circuit, a second input that is coupled to the output of the second flip-flop circuit, and an output that is coupled to a clear input of the first flip-flop circuit, and further coupled to a clear input of the second flip-flop circuit.

19. The circuit of Claim 18, wherein the clear logic circuit includes:

Application No. (if known): 10/804,866 Attorney Docket No.: 08211/0200390-US0

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